REMARKS

I. Introduction

Claims 1-5 and 10-14 are rejected, as set forth below. Applicants respectfully submit that the claims, as previously filed, are in condition for allowance and respectfully request reconsideration in view of the following.

Applicants also note that the current Office action is a final Office action. However, the current Office action includes new grounds for rejection. Therefore, applicants request that the finality of the Office action be withdrawn and either a Notice of Allowance or a new non-final Office action be issued.

II. Rejections under 35 U.S.C. §103(e)

Applicants note that the Office action appears to erroneously reject claims 1-5 and 10-13 under 35 U.S.C. §102(e), as the basis for rejection comprises a two-reference combination. Therefore, for purposes of responding to the Office action, applicants have assumed that the intended rejection of claims 1-5 and 10-13 is based on obviousness.

Claims 1-5 and 10-13 are apparently rejected under 35 U.S.C. §103(a) as being obvious in view of U.S. Patent No. 6,983,398 to Prabhu (hereinafter "*Prabhu*") and U.S. Publication No. 2004/0111653 to Arimilli et al. (hereinafter "*Arimilli*"). According to the Office action, *Prabhu* discloses all of the limitations of claims 1-5 and 10-13, except for (according to the Office action) disclosing that "a user of the system initiates the test control in order to perform the first self test process." Therefore, the Office action combined the teachings of *Prabhu* and *Arimilli* in an effort to yield all of the limitations of claims 1-5 and 10-13. Applicants have reviewed the Office action and respectfully submit that the claims, as previously filed, patentably distinguish over *Prabhu* in view of *Arimilli*.

Claim 1, upon which claims 2-5 depend, recites "[a] method for controlling the performance of self testing and extended self testing, the method performed by a system that includes a first self test process and a second self test process, the method performed by the system." The method includes "performing the first self test process in response to a first actuation of a test control by a user of the system." The method also includes "performing the second self test process in response to a second actuation of the test

control prior to lapse of a first predefined period of time." The method further includes "terminating the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time."

Claim 10, upon which claims 11-14 depend, recites "[a] system comprising a first processor that performs a first self test process in response to a first actuation of a provided test control by a user of the system." The system also includes "a second processor that performs the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time and terminates the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time."

As outlined below, *Prabhu* and *Arimilli* do not disclose, teach or suggest each of the limitations of claims 1-5 and 10-13.

For support of the rejection of claims 1-5 and 10-13, the Office action cites to column 3, lines 22-27 and column 5, line 64 to column 6, line 32 from *Prabhu*, each of which are reproduced below, respectively, for the Examiner's convenience:

> One or a set of various processors 110 tests one or a set of processors 110. One processor 110 may perform some tests while a processor 110 compares and analyzes the test results. Consequently, testing chip 100 may be referred to as "self-test" because chip 100 conducts tests using its own elements. (See column 3, lines 22-27 of *Prabhu*)

> In one embodiment, a processor 110 executes its corresponding test program independent of other processors. Each processor 110 starts and/or stops its program any time, at irregular intervals, and/or without other processors knowing about it, as long as the test results are available to be analyzed when analyzing the test results starts. The processors' system clocks do not have to be cycle locked, e.g., one clock does not depend on another clock, etc. For example, a processor 110-1 may run its program in series or in parallel with a processor 110-2; processor 110-1 may stat at time t1 and stop at time t2 while processor 110-2 starts at time t3 and stops at time t4 wherein times t1, t2, t3, and t4 are different and independent of one another, etc. However, t1 is less than or equal to t2. Similarly, t3 is less than or equal to t4. Since, in one embodiment, each processor 110 corresponds to a test program and each test program can provide different tests, one processor 110 can run different tests from another processor 110

> or analyze test results provided by other processors 110. For example, a processor 110-1 is testing a floating-point unit for a processor 110-2, while a processor 110-3 is testing an integer unit for a processor 110-4, and processor 110-5 compares the test results provided by processors 110-2 and 110-3, etc. In one embodiment, once a processor 110 finishes its test program, that processor sets a flag at a corresponding memory location so that other processors can take appropriate actions. For example, once each processor 110-1 and 110-2 finishes testing processor 110-3, each processor 110-1 and 110-2 sets a flag corresponding to the programs that each has executed. Processor 110-4, recognizing the flags of processors 110-1 and 110-2 have been set, starts running its program to analyze the test results provided by these processors 110-1 and 110-2. In an alternative embodiment, a processor 110 sets a flag when some portions of the test programs were executed so that the completed test results may be analyzed while additional tests are being executed. (See column 5, line 64 to column 6, line 32 of *Prabhu*)

The Office action also cites to paragraph 0117 of *Arimilli* disclosing that the "execution of the manufacturing test program can be initiated by the user, the operating system, or the hypervisor."

Applicant submits that the combination of *Prabhu* and *Arimilli* does not disclose, teach or suggest each of the limitations of claims 1-5 and 10-13. Claims 1-5, in part, recite "terminating the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time." Claims 10-13, in part, recite "a second processor that performs the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time and terminates the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time." *Prabhu* does not disclose, teach or suggest these features.

As noted above, column 5, line 64 to column 6, line 32 of *Prabhu,* which is cited in the Office action, discloses that each processor 110 starts and/or stops its program any time, at irregular intervals, and/or without other processors knowing about it, as long as the test results are available to be analyzed when analyzing the test results starts. There is no disclosure, teaching or suggestion in the cited sections of *Prabhu* of "terminating the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second

predetermined period of time," as recited in claims 1-5. There is also no disclosure, teaching or suggestion in *Prabhu* of "a second processor that performs the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time and terminates the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time," as recited in claims 10-13.

While the cited sections of *Prabhu* disclose that each processor starts and/or stops its program any time, as long as the test results are available to be analyzed when analyzing the test results starts, *Prabhu* does not disclose, teach or suggest "terminating the second self test process in response to a third actuation of the test control by the user of the system," as recited in the pending claims 1-5 (and similarly in claims 10-14). *Prabhu* also does not disclose, teach or suggest that "the third actuation is maintained for more than a second predetermined period of time," as recited in the pending claims 1-5 (and similarly in claims 10-14).

Arimilli does not cure any of the deficiencies of *Prabhu*, as outlined above. Specifically, *Arimilli* does not disclose, teach or suggest "terminating the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time," as recited in claims 1-5. *Arimilli* also does not disclose, teach or suggest "a second processor that performs the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time and terminates the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time," as recited in claims 10-13.

Based on the distinctions noted above, applicants request that the rejection under 35 U.S.C. §103(a) be withdrawn, because neither *Prabhu* nor *Arimilli,* whether taken singly or combined, discloses, teaches or suggests each of the limitations of claims 1 and 10. Each of claims 2-4 and 11-13 depend on claims 1 and 10, respectively, and should be allowed at least because of their dependence on claims 1 and 10.

Claim 14 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Prabhu* in view of *Arimilli* and U.S. Publication No. 2006/0273929 to Tran (hereinafter "*Tran*"). According to the Office action *Prabhu* and *Arimilli* disclose all of the limitations of claim 14, except for disclosing that "the first processor performs a traffic collision avoidance function and the second processor performs a terrain collision avoidance function." Therefore, the Office action combined the teachings of *Prabhu, Arimilli* and *Tran* in an effort to yield all of the limitations of claim 14. Applicants have reviewed the Office action and respectfully submit that claim 14, as previously filed, patentably distinguishes over *Prabhu* in view of *Arimilli* and *Tran*.

Paragraph 0009 of *Tran* discloses:

> The present invention processes navigation data, terrain data, air data and radar altitude, along with a hybrid avoidance solution generated by the Hybrid Air Collision Avoidance System to determine if there is a conflict in the ground domain. If there is a conflict, the specific information of location, avoidance maneuver path and time markers will be routed to the Hybrid Air Collision Avoidance System (HACAS). This information will allow the HACAS to verify the solution compatibility with the operating air traffic environment. If the feedback data identifies a positive in-compatibility condition found in the ground solution, then the system will apply the memorized trace process with the specific feedback information to refine the avoidance solution. If the revised solution is again verified, it takes the feedback data of predicting ground collision and provides a cross-feed of collision and avoidance data produced by the two avoidance modules by implanting unique air avoidance capabilities in the hybrid terrain collision avoidance engine and unique ground avoidance capabilities in the hybrid air collision avoidance module, along with the arbitration and controlling capability in the obstacle avoidance management module, which results in producing an obstacle solution.

Applicants respectfully submit that the combination of *Prabhu, Arimilli* and *Tran* does not disclose, teach or suggest each of the limitations of claim 10, upon which claim 14 depends. Specifically, *Tran* also does not disclose, teach or suggest "a second processor that performs the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time and terminates the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time," as recited in claim 10, upon which claim 14 depends.

Based upon at least the distinctions noted above, applicants request that the rejection under 35 U.S.C. §103(a) be withdrawn because neither *Prabhu, Arimilli* nor *Tran,* whether taken singly or combined, discloses, teaches or suggests each of the limitations of claim 10. Claim 14 depends on claim 10 and should be allowed at least because of its dependence on claim 10.

As previously noted, all of claims 1-5 and 10-14 recite subject matter which is not disclosed or suggested in the cited prior art references. Applicants, therefore, respectfully request that all of the pending claims be allowed.

CONCLUSION

Reconsideration is respectfully requested. Applicants believe the case is in condition for allowance and respectfully request withdrawal of the rejections and allowance of the pending claims.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to **Deposit Account No. 19-3878**.

The Examiner is invited to telephone the undersigned at the telephone number listed below if it would in any way advance prosecution of this case.

Respectfully submitted,

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